STP5NK100Z - STF5NK100Z STW5NK100Z

N-CHANNEL 1000V - 2.7Ω - 3.5A TO-220/TO-220FP/TO-247 Zener-Protected SuperMESH™MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STF5NK100Z	1000 V	< 3.7 Ω	3.5 A (*)	30 W
STP5NK100Z	1000 V	< 3.7 Ω	3.5 A	125 W
STW5NK100Z	1000 V	< 3.7 Ω	3.5 A	125 W

- TYPICAL R_{DS}(on) = 2.7 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES

Figure 1: Package

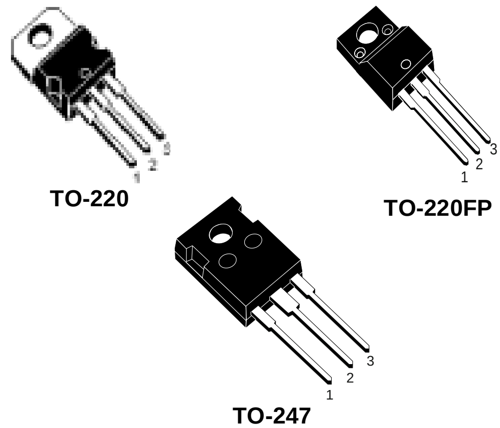


Figure 2: Internal Schematic Diagram

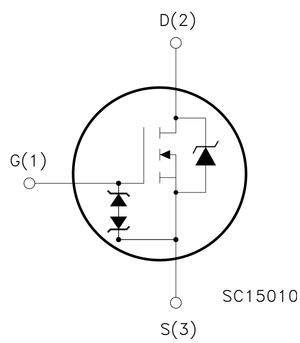


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STF5NK100Z	F5NK100Z	TO-220FP	TUBE
STP5NK100Z	P5NK100Z	TO-220	TUBE
STW5NK100Z	W15NK100Z	TO-247	TUBE

Rev. 2

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		STP5NK100Z STW5NK100Z	STF5NK100Z	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	1000		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	1000		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain Current (continuous) at T_C = 25°C	3.5	3.5 (*)	A
I_D	Drain Current (continuous) at T_C = 100°C	2.2	2.2 (*)	A
I_{DM} (•)	Drain Current (pulsed)	14	14 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	125	30	W
	Derating Factor	1	0.24	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	4000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		°C °C

(●) Pulse width limited by safe operating area
(1) I_{SD} ≤3.5A, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220 TO-247	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	1	4.2	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	3.5	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	250	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 7: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	1000			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125°C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 1.75 A		2.7	3.7	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V , I_D = 1.75 A		4		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		1154 106 21.3		pF pF pF
$C_{oss\ eq}$ (3).	Equivalent Output Capacitance	V_{GS} = 0 V, V_{DS} = 0 to 800 V		46.8		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	V_{DD} = 500 V, I_D = 1.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 21)		22.5 7.7 51.5 19		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 800 V, I_D = 3.5 A, V_{GS} = 10 V (see Figure 24)		42 7.3 21.7	59	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				3.5 14	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 3.5 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 3.5 A, di/dt = 100 A/µs V_{DD} = 35V (see Figure 22)		605 3.09 10.5		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 3.5 A, di/dt = 100 A/µs V_{DD} = 35V, T_j = 150°C (see Figure 22)		742 4.2 11.2		ns µC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.
(3) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Figure 3: Safe Operating Area For TO-220

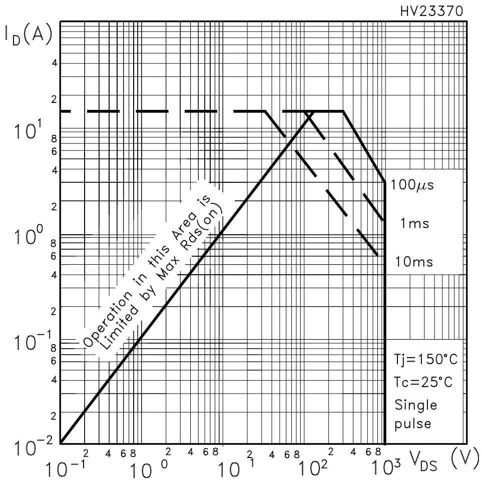


Figure 6: Thermal Impedance TO-220

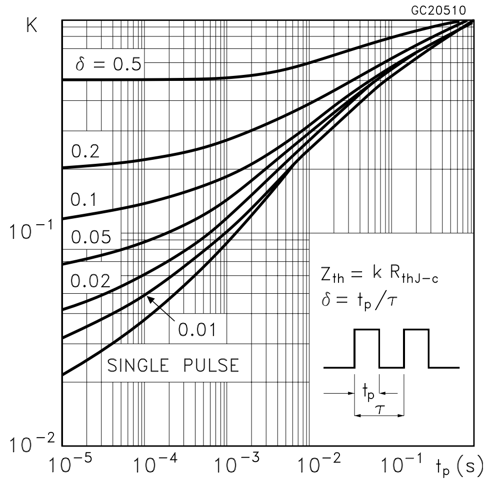


Figure 4: Safe Operating Area For TO-220FP

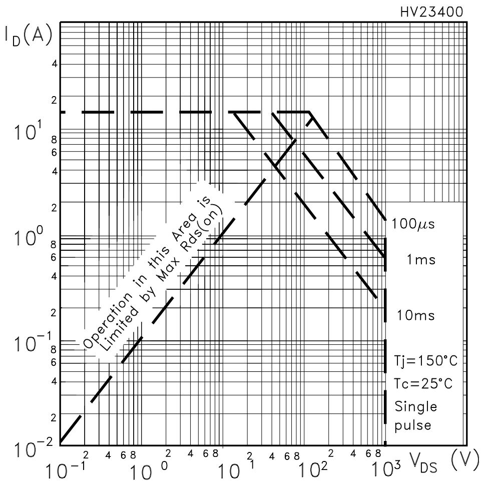


Figure 7: Thermal Impedance For TO-220FP

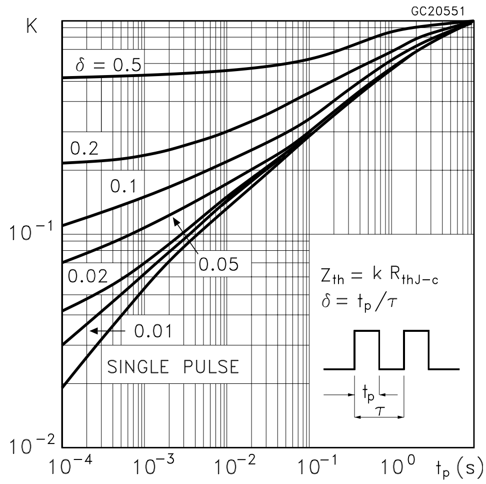


Figure 5: Safe Operating Area For TO-247

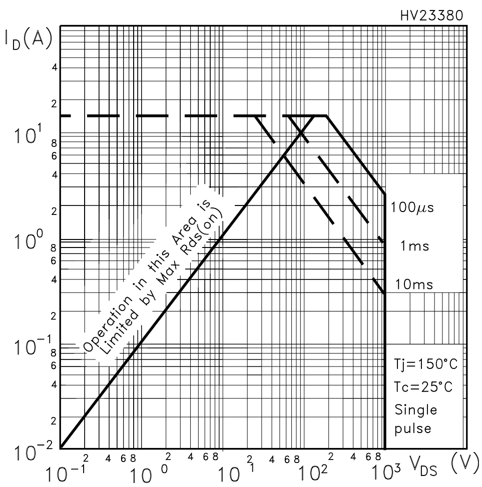


Figure 8: Thermal Impedance For TO-247

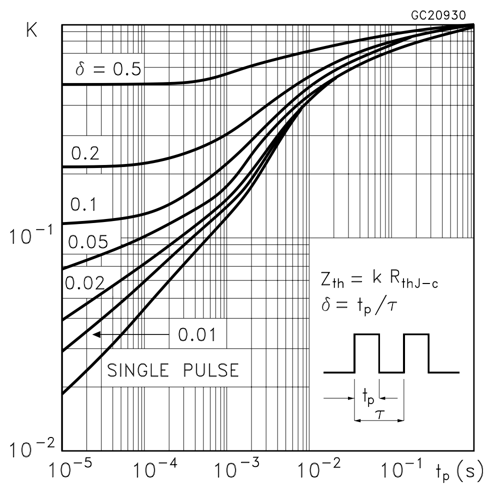


Figure 9: Output Characteristics

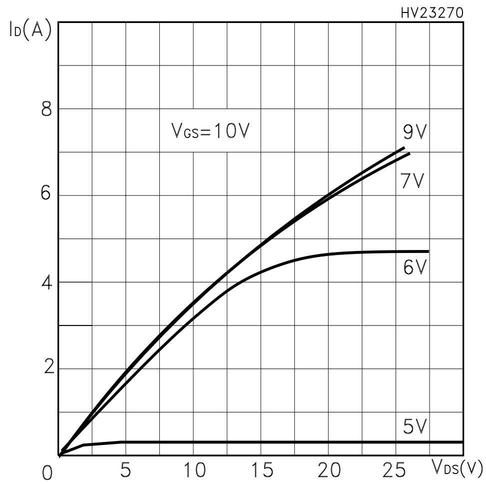


Figure 12: Transfer Characteristics

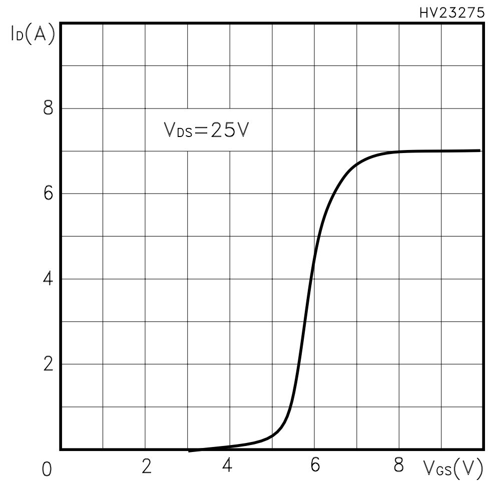


Figure 10: Transconductance

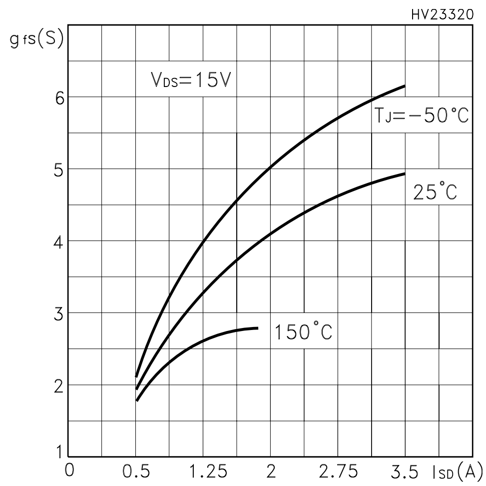


Figure 13: Static Drain-Source On Resistance

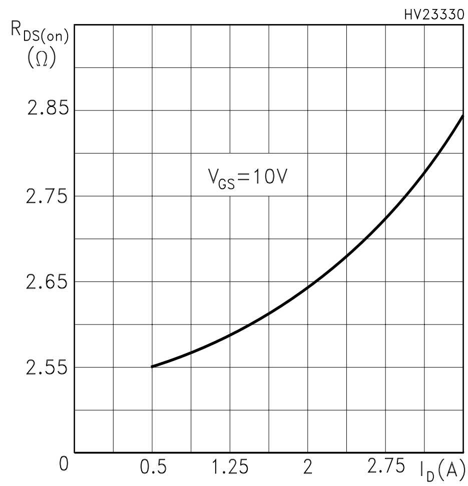


Figure 11: Gate Charge vs Gate-source Voltage

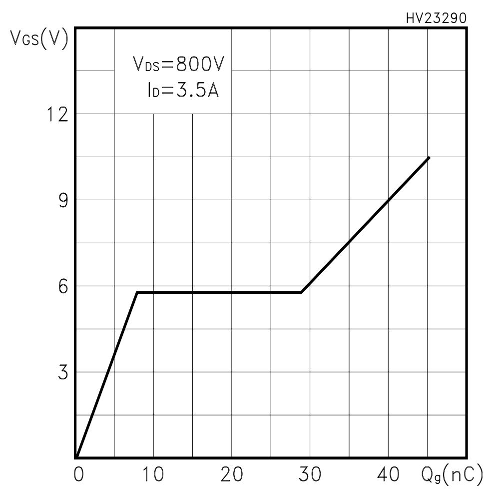


Figure 14: Capacitance Variations

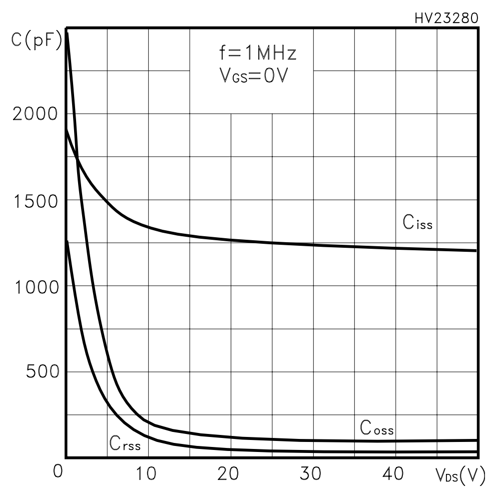


Figure 15: Normalized Gate Threshold Voltage vs Temperature

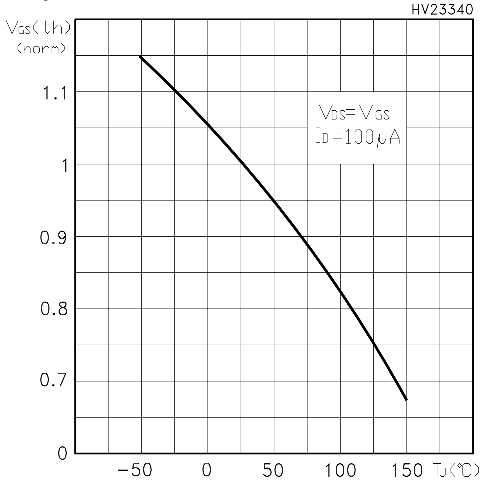


Figure 16: Source-Drain Forward Characteristics

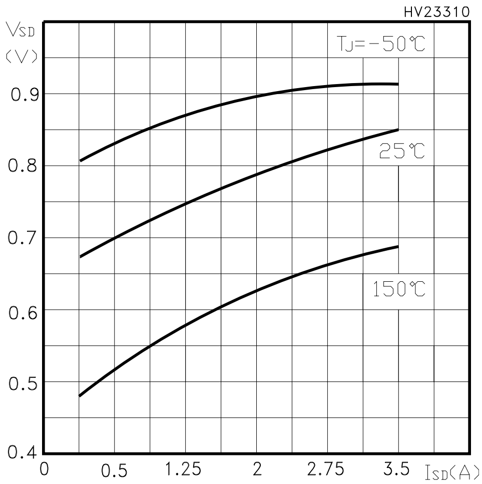


Figure 17: Maximum Avalanche Energy vs Temperature

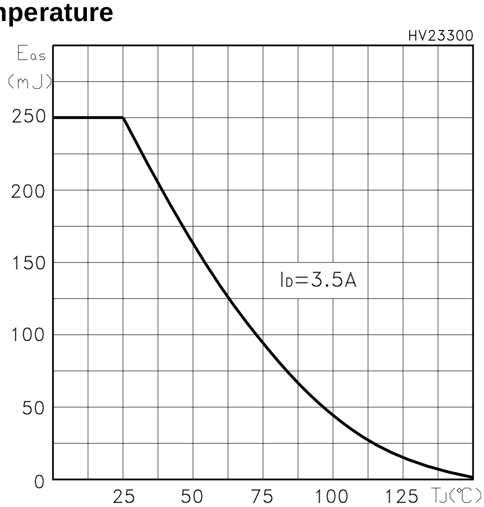


Figure 18: Normalized On Resistance vs Temperature

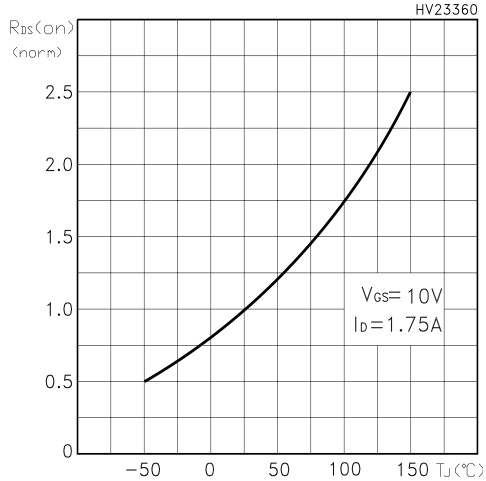


Figure 19: Normalized BV_{DSS} vs Temperature

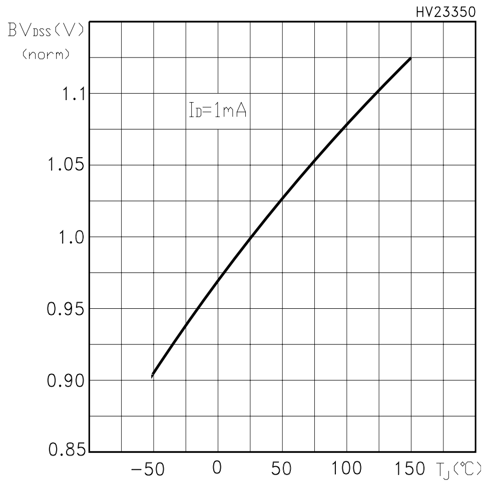


Figure 20: Unclamped Inductive Load Test Circuit

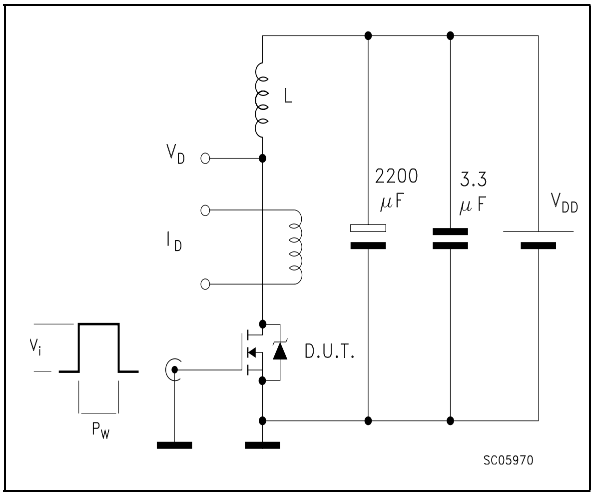


Figure 21: Switching Times Test Circuit For Resistive Load

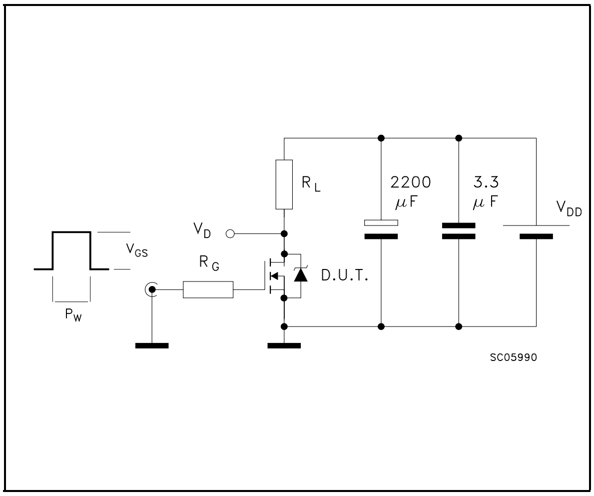


Figure 22: Test Circuit For Inductive Load Switching and Diode Recovery Times

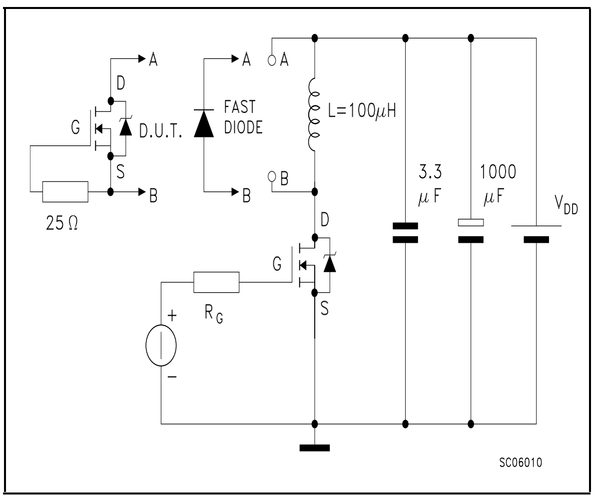


Figure 23: Unclamped Inductive Wafeform

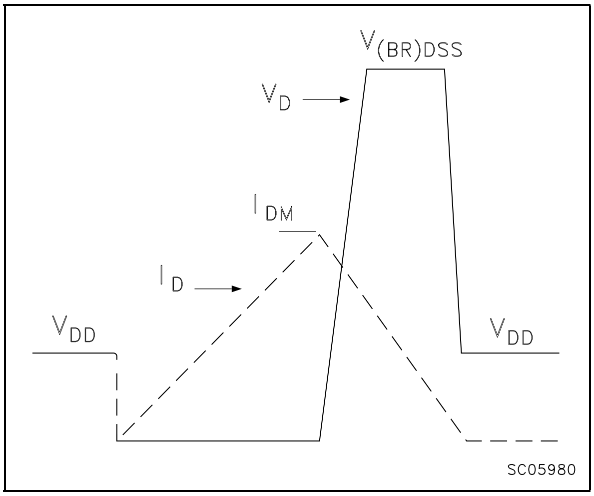
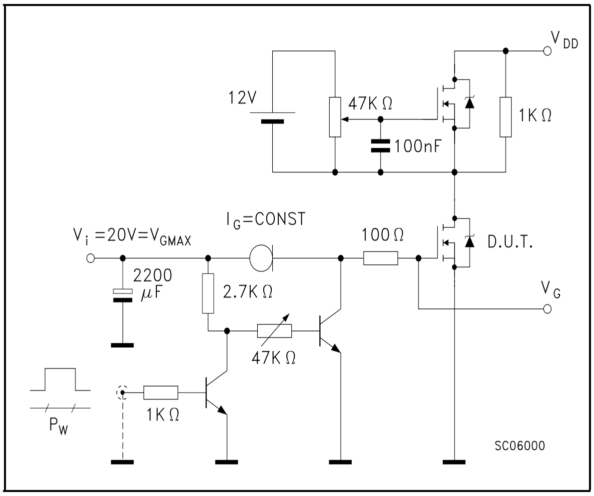
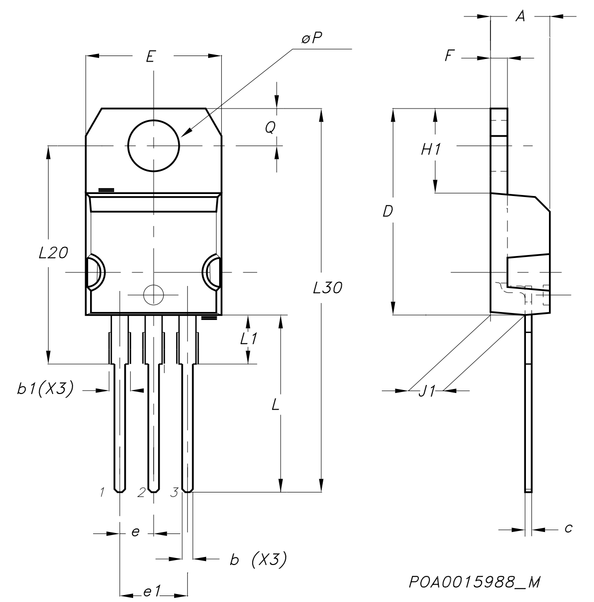


Figure 24: Gate Charge Test Circuit



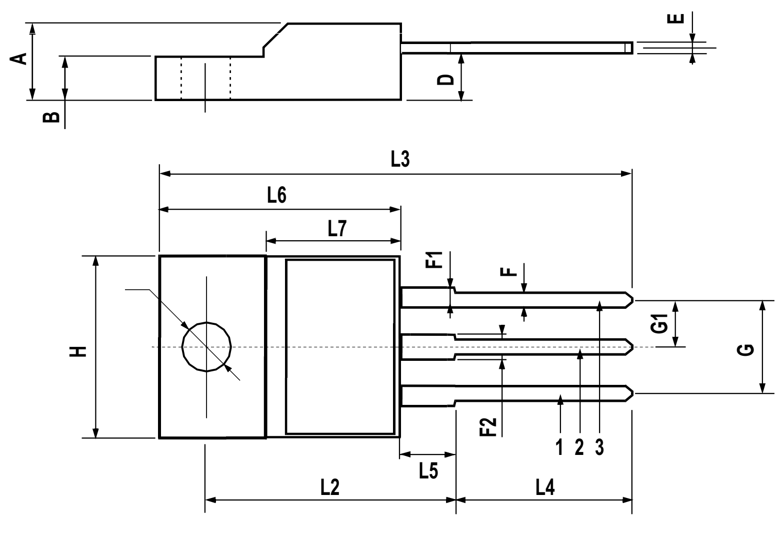
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	

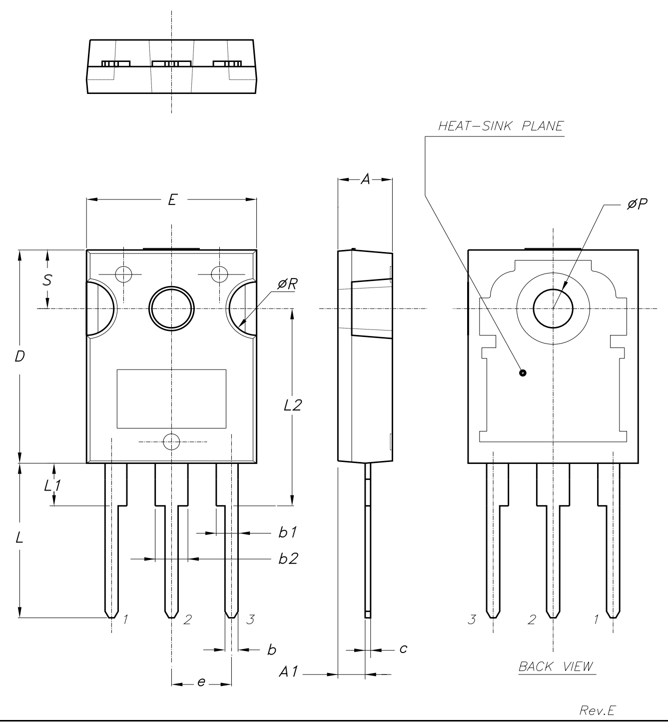


Table 10: Revision History

Date	Revision	Description of Changes
27-Sep-2004	1	First release.
08-Oct-2004	2	Final datasheet